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Autodesk Acuity on PC /.1. Field of the Invention The present invention relates generally to semiconductor memory devices, and more specifically to a semiconductor memory device having a test mode controller. 2. Description of the Related Art Semiconductor memory devices may include two types of fail bit map. One is a failure map which is a map table obtained by a test, in which memory cells storing data "0" are set to be test fail bits, and the other is a spare map which is a map table obtained by a process of actually testing defective memory cells. The fail bit map can be changed depending upon a level of a power supply voltage applied to the memory device. It is therefore desirable that the fail bit map is changed depending upon a power supply voltage which is supplied to the memory device of the burst I/O type performs a test on a core region, and a system is disconnected from the core region after completion of the test. As a result, while a fail bit map is being changed, data which should be stored in the memory cells is destroyed on an LSI chip. Since a memory cell for storing data having a predetermined value must be present for each word line (WL), the fail bit map table is provided on an LSI chip. Since a memory cell for storing data having a predetermined value must be present for each word line (WL). The fail bit map table is provided on an LSI chip. Since a memory cell for storing data having a predetermined value must be present f

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